

**IN THE CLAIMS**

**This listing of claims will replace all prior versions, and listings, of claims in the application:**

**Listing of Claims:**

1. (Currently amended) A packet formatter comprising:

a first processing block for receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, the robust stream comprising a plurality of robust packets each having associated therewith header bytes and parity bytes, locations of the parity bytes of a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bitstream signal;

a second processing block for determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame, said first processing block, in response to the determined locations of the parity bytes within each robust packet, removing the header bytes and parity bytes from the dual bitstream signal to output a first output signal; and

a third processing block for receiving said first output signal, said third processing block removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal; ~~and that is output from a data path output of said packet formatter~~

a fourth processing block for receiving said second output signal and producing

therefrom transport packets that are an output of said packet formatter, said fourth processing block comprising a data de-randomizer block for de-randomizing bytes associated with said standard and robust streams, and a delay calculation block for determining a delay associated with the robust stream with respect to a field synchronization signal, and applying a control signal to said data de-randomizer block to cause the data de-randomizer block to suspend its operation associated with said robust stream for a portion of a field in accordance with the determined delay.

2. (Currently amended) The packet formatter as set forth in claim 1 wherein said packet formatter passes bytes associated with said standard stream to said ~~data-path-output-of said packet formatter~~ first output signal after delaying said standard stream bytes by a predetermined delay time.

3. (Canceled)

4. (Currently amended) The packet formatter as set forth in claim 1, wherein ~~said second processing block is further capable of determining locations of said header bytes in said robust stream.~~

5. (Previously presented) The packet formatter as set forth in claim 1 wherein said second processing block includes a look-up table which identifies the locations of the parity bytes

for each robust packet depending upon the position of the robust packet within the frame.

6. (Previously presented) The packet formatter as set forth in claim 5 wherein said packet formatter generates and outputs packet identification information used by subsequent processing blocks following said packet formatter.

7. (Previously presented) A signal comprising the second output signal output from the data path output of the packet formatter as set forth in claim 1.

8. (Currently amended) For use in a television receiver capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, the robust stream comprising a plurality of robust packets each having associated therewith header bytes and parity bytes, locations of the parity bytes of a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bitstream signal, a method comprising acts of:

receiving in a packet formatter said dual bitstream signal;

determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame;

removing the header bytes and parity bytes from the dual bitstream signal to thereby produce a first output signal; and

removing from said first output signal duplicate bits associated with said robust

stream to thereby produce a second output signal; ~~that is output from a data path output of~~  
said packet formatter

de-randomizing bytes of said second output signal associated with said standard  
and robust streams to produce a data path output of said packet formatter;

determining a delay associated with the robust stream with respect to a field  
synchronization signal; and

applying a control signal to suspend said data de-randomizing act associated with  
said robust stream for a portion of a field in accordance with the determined delay.

9. (Currently amended) The method as set forth in claim 8 further comprising ~~the step~~an  
act of delaying bytes associated with said standard stream by a predetermined delay time  
before outputting said delayed standard stream bytes on said data path output of said  
packet formatter.

10. (Canceled)

11. (Currently amended) The method as set forth in claim 8 further comprising ~~the step~~an  
act of determining locations of the header bytes in said robust stream.

12. (Currently amended) The method as set forth in claim 8 wherein said ~~step~~act of  
determining the locations of said parity bytes comprises ~~the step~~an act of determining the  
locations of said parity bytes from a look-up table which identifies the locations of the parity

bytes for each robust packet depending upon the position of the robust packet within the frame.

13. (Currently amended) The method as set forth in claim 12 further comprising the steps of generating and outputting packet identification information used by subsequent processing blocks following said packet formatter.

14. (Canceled)

15. (Currently amended) A television receiver comprising:

receiver front-end circuitry capable of receiving and down-converting a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream comprising a plurality of robust packets each having associated therewith header bytes and parity bytes, locations of the parity bytes of a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bitstream signal, the receiver front-end circuitry producing a baseband signal; and

a forward error correction section capable of receiving said baseband signal from said receiver front-end circuitry, said forward error correction section comprising:

a packet formatter comprising:

a first processing block for receiving said standard stream and said robust stream associated with said baseband signal,

a second processing block for determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame, said first processing block, in response to the determined locations of the parity bytes within each robust packet, removing the header bytes and parity bytes from the dual bitstream signal to output a first output signal, and

a third processing block for receiving said first output signal, said third processing block removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter;

a robust deinterleaver for receiving the second output signal, and deinterleaving data in the robust stream to output a third output signal;

a Reed-Solomon decoder for receiving the third output signal, and decoding data in the third output signal to output a fourth output signal; and

a derandomizer for receiving the fourth output signal and derandomizing bytes associated with said standard stream and bytes associated with said robust stream; and

a delay calculation block for determining a delay associated with the robust stream with respect to a field synchronization signal, and applying a control signal to said data de-randomizer to cause the data de-randomizer to suspend its operation associated with said robust stream for a portion of a field in accordance with the determined delay.

16. (Previously presented) The television receiver as set forth in claim 15 wherein said packet formatter passes bytes associated with said standard stream to said data path

output of said packet formatter after delaying said standard stream bytes by a predetermined delay time.

17. (Canceled)

18. (Previously presented)The television receiver as set forth in claim 15 wherein said second processing block further determines the locations of said header bytes in said robust stream.

19. (Previously presented)The television receiver as set forth in claim 18 wherein said second processing block comprises a look-up table which identifies the locations of the parity bytes for each robust packet depending upon the position of the robust packet within the frame.

20. (Previously presented)The television receiver as set forth in claim 19 wherein said packet formatter generates and outputs packet identification information used by subsequent processing blocks following said packet formatter.

21. (Canceled)

22. (Previously presented)A data de-randomizer for use in a television receiver capable of receiving a dual bitstream signal comprising a standard stream compatible with the

Advanced Television Systems Committee (ATSC) standard and a robust stream, said data de-randomizer comprising:

a standard de-randomizer for de-randomizing bytes associated with said standard stream; and

a robust de-randomizer for de-randomizing bytes associated with said robust stream,

wherein said data de-randomizer further comprises a delay calculation circuit for determining a delay associated with the robust stream with respect to a field synchronization signal, and applying a control signal to the robust de-randomizer to cause the robust de-randomizer to suspend its operation for a portion of a field in accordance with the determined delay.

23. (Previously presented)The packet formatter of claim 1, wherein locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame, and wherein the second processing block is capable of determining the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame.

24. (Previously presented)The method of claim 8, wherein locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame, and wherein



determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame comprises determining the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame.

25. (Previously presented)The television receiver of claim 15, wherein locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame, and wherein the second processing block determines the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame.

26. (Previously presented)The data de-randomizer of claim 22, further comprising a multiplexer receiving de-randomized bytes associated with said standard stream from the standard de-randomizer, and receiving de-randomized bytes associated with said robust stream from the robust de-randomizer, and multiplexing the de-randomized bytes associated with said standard stream from the standard de-randomizer with the de-randomized bytes associated with said robust stream from the robust de-randomizer.

27. (Previously presented)The data de-randomizer of claim 22, wherein the delay calculation circuit includes a look-up table storing values that are used to determine the delay.